What is claimed is:

1. A phase-locked loop frequency synthesizer comprising:

a phase/frequency detector that compares a reference frequency with an output frequency signal and generates an appropriate charge pump control voltage;

a charge pump coupled to said phase/frequency detector that generates a loop filter control current from the charge pump control voltage;

a loop filter coupled to said charge pump that generates a loop filter voltage;

an oscillator bank coupled to the loop filter comprising a plurality of voltage controlled oscillators;

a feedback circuit coupled between said oscillator bank and said phase/frequency detector that provides the output frequency signal to the phase/frequency detector; and

a logic interface coupled to said oscillator bank for enabling one of said voltage controlled oscillators at a time.

2. The phase-locked loop frequency synthesizer of claim 1, wherein the phase-locked loop frequency synthesizer is integrated on a single chip, and said loop filter is a line out to off-chip capacitors and resistors.

3. The phase-locked loop frequency synthesizer of claim 1, wherein the phase-locked loop frequency synthesizer is integrated on a single semiconductor chip with bi-polar components.

4. A local oscillator integrated on a single semiconductor chip having a reference frequency input and a frequency output, comprising:

a phase-locked loop for comparing the difference in phase between the reference frequency input and the frequency output of the local oscillator, wherein said phase-locked loop includes an oscillator bank;

said oscillator bank comprising a plurality of voltage controlled oscillators connected in parallel; and

a logic interface coupled to said oscillator bank for enabling one of said voltage controlled oscillators at a time.

5. The local oscillator of claim 4, further comprising:

a frequency divider coupled to the reference frequency input and said phase-locked loop for dividing the reference frequency input to obtain a new reference frequency; and

said logic interface is coupled to said frequency divider for enabling programming of the new reference frequency.

6. The local oscillator of claim 4, wherein said phase-locked loop includes a frequency divider for changing the frequency output before comparison with the reference frequency input, and wherein said logic interface is coupled to said frequency divider for enabling programming of the output frequency.

7. The local oscillator of claim 4, wherein said phase-locked loop includes a loop filter implemented by a line out to off-chip capacitors and resistors.

8. A direct down-conversion broadband tuner integrated on a single semiconductor chip comprising:

at least one mixer;

at least one low-pass filter;

at least one amplifier; and

a local oscillator comprising:

a phase-locked loop for comparing the difference in phase between a reference frequency input and a frequency output from the local oscillator, wherein said phase-locked loop includes an oscillator bank;

said oscillator bank comprising a plurality of voltage controlled oscillators connected in parallel; and

a logic interface coupled to said phase-locked loop for enabling one of said voltage controlled oscillators at a time.

9. The direct down-conversion broadband tuner of claim 8, further comprising:

a frequency divider coupled to the reference frequency input and said phase-locked loop for dividing the reference frequency input to obtain a new reference frequency; and

said logic interface is coupled to said frequency divider for enabling programming of the new reference frequency.

10. The direct down-conversion broadband tuner of claim 8, wherein said phase-

locked loop includes a frequency divider for changing the frequency output before comparison with the reference frequency input, and wherein said logic interface is coupled to said frequency divider for enabling programming of the output frequency.

11. The direct down-conversion broadband tuner of claim 8, wherein said phase-locked loop includes a loop filter implemented by a line out to off-chip capacitors and resistors.

12. A method for providing a local oscillator integrated on a single semiconductor chip for use in a broadband tuner, comprising the steps of:

providing a phase-locked loop having an oscillator bank comprising a plurality of voltage controlled oscillators;

connecting a logic interface to the oscillator bank such that each of the voltage controlled oscillators can be selectively enabled to the exclusion of the other voltage controlled oscillators; and

programming the logic interface such that an appropriate voltage controlled oscillator is enabled when a carrier frequency is selected.

13. The method of claim 12, wherein said connecting step further comprises connecting the logic interface to a frequency divider located inside the phase-locked loop, and wherein said programming step further comprises programming the logic interface to select an appropriate number to supply to the frequency divider based on an input reference frequency and the carrier frequency selected.

14. The method of claim 13, further comprising the steps of:

providing a reference frequency divider coupled to the phase-locked loop input;

connecting the logic interface to the reference frequency divider; and

programming the logic interface to select an appropriate number to supply to the reference frequency divider based on the input reference frequency and the selected carrier frequency.

15. The method of claim 14, further comprising the step of:

calibrating the oscillator bank to determine the appropriate number to supply to the reference frequency divider, the appropriate number to supply to the frequency divider and the appropriate voltage controlled oscillator to enable, based upon a set of carrier frequencies and the input reference frequency.

16. A method for providing a broadband tuner integrated on a single semiconductor chip comprising the steps of:

supplying at least one mixer, at least one low-pass filter and at least one amplifier;

providing a phase-locked loop having an oscillator bank comprising a plurality of voltage controlled oscillators;

connecting a logic interface to the oscillator bank such that each of the voltage controlled oscillators can be selectively enabled to the exclusion of the other voltage controlled oscillators; and

programming the logic interface such that an appropriate voltage controlled oscillator is enabled when a carrier frequency is selected.

17. The method of claim 16, wherein said connecting step further comprises connecting the logic interface to a frequency divider located inside the phase-locked loop, and wherein said programming step further comprises programming the logic interface to select an appropriate number to supply to the frequency divider based on an input reference frequency and the carrier frequency selected.

18. The method of claim 17, further comprising the steps of:

providing a reference frequency divider coupled to the phase-locked loop input;

connecting the logic interface to the reference frequency divider; and

programming the logic interface to select an appropriate number to supply to the reference frequency divider based on the input reference frequency and the selected carrier frequency.

19. The method of claim 18, further comprising the step of:

calibrating the oscillator bank to determine the appropriate number to supply to the reference frequency divider, the appropriate number to supply to the frequency divider and the appropriate voltage controlled oscillator to enable, based upon a set of carrier frequencies and the input reference frequency.

20. The method of claim 18, further comprising the steps of:

supplying a local oscillator output divider coupled to the mixer and the local oscillator;

connecting the logic interface to the local oscillator output divider; and

programming the logic interface to select an appropriate number to supply to the local oscillator output divider based on the input reference frequency and the selected carrier frequency.

21. The method of claim 20, further comprising the step of:

calibrating the oscillator bank to determine the appropriate number to supply to the reference frequency divider, the appropriate number to supply to the frequency divider, the appropriate number to supply to the local oscillator output divider and the appropriate voltage controlled oscillator to enable, based upon a set of carrier frequencies and the input reference frequency.

22. A method for calibrating a local oscillator, comprising a plurality of voltage controlled oscillators, integrated on a single semiconductor chip for use in a broadband tuner, comprising the steps of:

selecting an initial frequency;

checking a lock detect output of a phase-locked loop iteratively for frequencies above and below the initial frequency to determine a lower edge and an upper edge of a set of frequencies to which a current voltage controlled oscillator can be tuned; and

performing said selecting and checking steps for each voltage controlled oscillator.

23. The method of claim 22, wherein said checking step is performed using a binary search algorithm.

24. The method of claim 23, wherein the binary search uses an initial step size between ten and fifty percent of the predicted bandwidth of the current voltage controlled oscillator.

25. The method of claim 22, wherein said selecting step uses a predicted center frequency for the current voltage controlled oscillator.

26. The method of claim 22, further comprising the step of:

calculating breakpoints between each voltage controlled oscillator from a set of upper and lower edges thereby minimizing the probability of one of the voltage controlled oscillators being used to tune to a frequency near either the upper or lower edge of that voltage controlled oscillator's tuning range.

27. The method of claim 26, further comprising the step of:

generating a look-up table for identifying which voltage controlled oscillator to use given a specified carrier frequency.

28. The method of claim 27, wherein said generating step further comprises generating a set of divide ratios to apply to an output of the local oscillator for inclusion in the look-up table.

29. The method of claim 26, wherein said calculating step further comprises

calculating breakpoints for at least one pseudo voltage controlled oscillator.

30. The method of claim 29, further comprising the step of:

generating a look-up table for identifying which voltage controlled oscillator to use, and a divide ratio to apply to an output of the local oscillator, given a specified carrier frequency.

31. The method of claim 22, wherein the method is performed once at start-up.

32. A method for calibrating a local oscillator, comprising a plurality of voltage controlled oscillators, integrated on a single semiconductor chip for use in a broadband tuner, comprising the steps of:

selecting an initial frequency for one of the voltage controlled oscillators;

checking a lock detect output of a phase-locked loop iteratively for frequencies above and below the initial frequency to determine a lower edge and an upper edge of a set of frequencies to which the one voltage controlled oscillator can be tuned; and

calculating a lower and an upper edge for each of the remaining voltage controlled oscillators based on the upper and the lower edge of the one voltage controlled oscillator and a set of predicted center frequencies for the remaining voltage controlled oscillators.